Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **V IN**
2. **N/C**
3. **VIP**
4. **N/C**
5. **V –**
6. **OUT**
7. **V +**

**4 5 6**

**2 1 8 7**

**3**

**.033”**

**.057”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: FLOATING**

**Mask Ref: TI 14551**

**APPROVED BY: DK DIE SIZE .033” X .057” DATE: 6/15/18**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: OPA140A**

**DG 10.1.2**

#### Rev B, 7/1